Datapath

CSC 211.01 — Friday, October 30, 2015
Agenda Today

• Return exam 2
• Datapath Practice
• Review
  • Implementing Procedures
  • Addressing
  • Program Translation
Return Exam 2

• Weighted with a linear function \((y=mx+b)\)
Given the component latencies shown below, what is the latency for an ADD instruction?

A. 850ps  
B. 1150ps  
C. 1350ps  
D. 1450ps  
E. None of the above
Given the component latencies shown below, what is the latency for an ADDI instruction?

A. 1250ps
B. 1350ps
C. 1450ps
D. 1550ps
E. None of the above
Given the component latencies shown below, what is the latency for a SW instruction?

A. 1250ps
B. 1350ps
C. 1450ps
D. 1550ps
E. None of the above
Given the component latencies shown below, what is the latency for a LW instruction?

A. 1450ps
B. 1600ps
C. 1650ps
D. 1950ps
E. None of the above
Implementing Procedures

• Calling and returning
• Calling conventions (registers)
• Using the stack
Addressing

• Immediate (direct)
• Register (indirect)
• Displacement
• PC-relative
• Pseudodirect
Program Translation

- Compiler
- Assembler
- Linker
- Loader
- (Dynamic Linker)